In the Claims

The status of claims in the case is as follows:

We claim:

1. [Currently amended] A decoupling capacitor, comprising:

a fixed resistance in series with said capacitor, said capacitor formed by a polysilicon layer and a diffusion layer, said fixed resistance formed by contacts connecting said polysilicon layer to a first voltage level buss and said diffusion layer to a second voltage level buss; and

said contacts being of location ~~and quantity~~ and capacity for protecting surrounding circuits in the event there is a defect shorting said busses together by limiting defect current while allowing said capacitor to function at a frequency sufficiently high to suppress noise on said first and second busses to a value which achieves bus stability.

2. [Currently amended] The decoupling capacitor of claim 1, further comprising:

said contacts including a first set of contacts to a first voltage and a second set of contacts to a second voltage;

a defect leakage current limiting path including said first set and said second sets of contacts separated by a distance optimized to cause a defect shorting said ~~polysilicon gate~~ polysilicon layer to said substrate to force defect current to travel from said first set of contacts through a section of the substrate, then to the polysilicon through the defect, and then along the rest of the ~~polysilicon gate~~ polysilicon layer to said second set of contacts.

3. [Original] The decoupling capacitor of claim 2, further comprising:

said first set of contacts and said second set of

contacts determined in number and location to provide preselected minimum and maximum resistance values between said first and second sets of contacts, said minimum resistance value for achieving a preselected maximum leakage current through any defect site in said polysilicon layer, and said maximum resistance value for achieving a preselected overall decoupling RC factor sufficient for a minimum RC network bandwidth.

4. [Original] The decoupling capacitor of claim 3, further comprising providing said first and second sets of contacts in sufficient number to effectively achieve total contact resistance less than 10% of combined sheet resistance of said diffusion and polysilicon layers across a distance separating said first and second sets of contacts.

5. [Original] The decoupling capacitor of claim 2, further comprising providing N pairs of contacts in said sets of contacts and placing said first and second sets of contacts separated by a distance K sufficient to achieve a leakage limiting resistance of R and a bandwidth limiting resistance of R/2.

6. [Original] The decoupling capacitor of claim 2, further comprising providing a technology-dependent number of contacts selected in number sufficient to achieve total contact resistance less than 10% of combined sheet resistance of said diffusion and polysilicon layers across a distance separating said first and second sets of contacts.

7. [Withdrawn] A method for determining the number and position of contacts in a decoupling capacitor including a polysilicon layer and a diffusion layer, comprising:

determining a maximum allowable defect current I for IDDQ testing of said capacitor;

determining a minimum sheet resistance R to achieve said defect current I;

determining minimum distance K between first and second sets of said contacts to achieve said minimum sheet resistance R;

determining number of said contacts N in said sets of contacts to provide sufficiently low contact resistance to assure said minimum sheet resistance R dominates

total resistance between said first and second sets of contacts; and

providing in said decoupling capactior contact sites of sufficient area to accommodate N said contacts with said first and second sets of said contacts separated by at least distance K.

8. [Withdrawn] A program storage device readable by a machine, tangibly embodying a program of instructions executable by a machine to perform method steps for determining the number and location of contacts in a decoupling capacitor including a polysilicon layer and a diffusion layer, said method comprising:

determining a maximum allowable defect current I for IDDQ testing of said capacitor;

determining a minimum sheet resistance R to achieve said defect current I;

determining minimum distance K between first and second sets of said contacts to achieve said minimum sheet resistance R;

determining number of said contacts N in said sets of contacts to provide sufficiently low contact resistance to assure said minimum sheet resistance R dominates total resistance between said first and second sets of contacts; and

defining in said decoupling capacitor contact sites of sufficient area to accommodate N said contacts with said first and second sets of said contacts separated by at least distance K.